SSC DETECTOR R&D PROPOSAL

DEVELOPMENT OF TECHNOLOGY FOR PIXEL VERTEX DETECTOR

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1 Executive Summary

- **Proposal Objectives:**

  This proposal covers the first phase (12 months) of a 36 month program to demonstrate key technical performance requirements for silicon pixel vertex detectors for SSC. The effort addresses differing needs for high P_t and intermediate P_t experiments such as those studied by the SDE and BCD groups. During the first year, system design concepts will be developed, preliminary system cost analysis will be performed, and prototype hybrid detectors will be designed and fabricated. After the full 36 month term, final design verification and key hardware elements will be demonstrated; beam tests of detector arrays will demonstrate readiness for full scale engineering development.

- **Team Description:**

  The SSC places severe performance requirements upon detector technology, requiring new and imaginative solutions in many areas such as tracking and vertex detection. A team approach coupling the high energy physics community and industry is essential to establish realistic technical requirements, develop an appropriate systems architecture, provide rapid evaluation and test beam results, and optimize the overall system performance for an acceptable cost. The industrial partner, Hughes Aircraft Company, is a recognized leader in both pixel array design and sophisticated electronic system fabrication; the physics research members of the team combine technical expertise in semiconductor devices and extensive and varied experience in high energy physics research. The major SSC initiatives BCD and SDE reflecting this experience are well-represented in this collaboration.

- **Key Elements of Proposed Program:**

  - Early appraisal of cost and system feasibility issues reduces risk;
  - Early involvement of industry will increase rate of progress toward a final system and introduce sophisticated management practices;
  - First year effort addresses wide range of physics requirements;
  - Concentrated effort by all key members of physics community eliminates duplication of effort and ensures good communications.

2 Introduction

For the SSC, silicon pixel detectors offer the attractive prospect of highly effective pattern recognition, high spatial resolution, high radiation tolerance, and fast time response - essential qualities for vertex detection and tracking close to the beam pipe. The extremely challenging physics and background environment of the SSC would appear to make all other known detector concepts inferior to a pixel detector for this purpose. Much of the basic semiconductor technology needed to realize pixel detectors suitable for the SSC already exists, and significant advances in pixel detector designs have been achieved during the current SSC Generic R&D program. Nevertheless, to meet projected SSC schedules for detector construction, a substantial effort is needed now to realize the progress needed to achieve the required technical performance and to establish budgetary requirements for these detector systems.

Within the broadest context of SSC physics, there are perhaps three or four distinct categories for pixel detector applications. High P_t physics, with a wide variety of physics signatures, has of necessity a complex two-level trigger structure that has substantial impact on the pixel array architecture. Intermediate P_t physics, on the other hand, places emphasis on very rapid readout of detector information after a single relatively short trigger decision interval. A third category includes more specialized physics goals such as exotic particle searches where high quality ionization density information as well as spatial resolution is required. Finally, it has been recognized that the pixel arrays we intend to develop are very well matched to a possible solution (in conjunction with an image intensifier) for the rather daunting readout system requirements for scintillating fiber detector at the SSC. Only the first two categories are addressed directly in this proposal.

To address the need for rapid progress in the development of silicon pixel vertex detectors, a sizable collaboration including an experienced industrial partner has been formed. In large part, the proponents are associated with the "BCD" and "SDE" groups which have undertaken substantial efforts to evaluate the detector requirements for the intermediate and high P_t SSC physics contexts respectively. Through these associations, the technical goals

of this collaboration will maintain the closest possible relationship to the requirements associated with the high and intermediate P_t physics of the SSC. The collaboration has entered into a teaming agreement expressing our collective intention to work together through the construction phase of SSC detector systems.

The current proposal presents in detail our plan for the first year of what is foreseen as a three year program to reach a rather complete engineering demonstration. The development program for the following two years, including an approximate estimate of budgetary requirements, is given in broad outline.

3 Relevance of Pixel Vertex Technology to the SSC

3.1 Overview

The SSC will provide a window into an entirely new and uncharted physics domain. In order to best exploit the discovery potential of this instrument, interactions must be studied in sufficient detail to separate rare or unexpected processes from the ferocious backgrounds characteristic of the SSC. New physics processes are expected to generate heavy quarks and leptons as decay products much more frequently than known QCD processes. Heavy quarks will be copiously produced, offering an opportunity for the study of the mechanism of CP violation and rare decays. On a more mundane level, a consequence of the design luminosity is a high probability of more than one interaction per beam crossing. It is clear that the ability to measure vertex structure is an essential although extremely difficult technical challenge.

3.2 Intermediate P_t Physics and Vertex Detection

The BCD experiment is a program of physics that will study intermediate and low P_t physics at the SSC. It is hoped that BCD can begin data taking at Fermilab in the mid 1990's, with some detector systems. The complete experiment will be a first round detector at the SSC. The physics goal of this experiment is the complete and thorough study of the CP violating decay modes of the B meson. Only B mesons that decay to all charged states are considered. CP violation has great importance within the standard model and is a subject of much interest for theorists and experimentalists. The following is a list of some of the interesting physics questions that can be addressed with a detector at the SSC that has a powerful vertex detector.

1. Cosmological models invoke CP to help explain the matter-antimatter asymmetry in the universe. Thus the existence of the universe is

thought to be related to CP in some way.

2. Multiple Higgs bosons can lead to relative complex phases that in turn have CP violating effects. Thus the understanding of mass generation and CP is related.

3. CP violation is important to the generation puzzle. With two families there is no CP violation in the Standard Model. All existing data is consistent with three families or one complex phase. If there are four families, then there are three complex phases and new CP phenomena are expected.

4. Measurements of CP violation in the B system can overconstrain the C-K-M matrix.

5. Left-right symmetric models predict small CP violating effects in the B system.

6. There is some hope that if the C-K-M elements are well determined it will be possible to observe symmetries in the mass matrices of the quarks and therefore Yukawa couplings.

7. The Standard Model is a parametrization of experimental data. It provides no insight into the origin of CP violation. Further study of CP violation in the K system and information from a new system may provide valuable information far beyond the standard model.

8. The search for Higgs particles that decay into $\bar{b}b$ is made possible with a vertex detector. Technicolor mesons can decay to $\bar{b}b$ as well.

9. In summary, many fundamentally important physics topics are within reach of study at the SSC if a vertex detector of sufficient performance can help extract the B signal.

3.2.1 BCD Vertex Detector

Introduction The emerging opportunities to study B physics at the SSC are primarily as a result of the advancement of silicon vertex detector technology. It has been understood for sometime that the SSC could produce of

order 10^{12} $\bar{b}b$ pairs per year. The experimental challenge is to fully reconstruct the B meson invariant mass from its decay products. There are 2-6 charged tracks from the B meson and typically over 100 charged tracks in the event. Fortunately the B lifetime is sufficiently long that the decay vertex can be separated from the beam collision point using a precision vertex detector. The invariant mass is then calculated using only tracks coming from a secondary vertex. Techniques like this have given rejection factors of up to 10^6 in some decay channels in low rate fixed target experiments.

There exists to date no silicon vertex detector in an e^+e^- machine or hadron collider, though efforts are underway to install such devices in several experiments, like CDF at Fermilab, MarkII at SLAC, Delphi and Aleph at CERN. These first generation detectors all use silicon strip technology and newly developed VLSI circuits mounted on the detector for amplification and readout processing. The SLD vertex detector at SLAC will be a CCD device with very slow readout.

The most relevant work for BCD is that of the CDF group. However, in order to reconstruct fully the B meson mass with high efficiency over a large solid angle, the BCD vertex detector design is significantly more complex. The requirements are described in the following sections.

Philosophy of BCD Vertex Detector The BCD must build the best vertex detector possible if it is to achieve success at the SSC. If the vertex detector does not work well, the experiment will be severely compromised.

The bump bonded pixel vertex detector can be considered the ultimate device if the design specifications can be achieved. Due to the large number of channels associated with a pixel device, a hybrid of pixels and strips may be necessary. Pursuing the development of pixels at this time allows the maximum in flexibility in the design of the vertex detector system and inner tracking layers. Much research has been performed by Arens et al., Nygren et al., and Parker et al.. This proposal represents the beginnings of the development stage of a pixel detector.

Vertex Detector Requirements The BCD vertex detector should determine the impact parameter of charged tracks with respect to the decay vertex to less than $10\mu m$ rms error. The multiple scattering error on the track is proportional to $R/P_t\sqrt{L/L_0}$, where R is the radius to the first detector plane, P_t is the transverse momentum and L/L_0 is the percent radiation length. To meet the required resolution goals, the vertex detector inner layer must be placed at R$\sim$ 1.25 cm. This is because the average P_T of tracks from B decay at the SSC is less than 1 GeV/c. Furthermore, there is much incentive to minimize the amount of material and the Z of the material. Beryllium is therefore a common choice for the support material.

The minimal radiation damage tolerance for gamma rays is 10Mrads. If luminosities above $10^{32}cm^{-2}sec^{-1}$ are required to study smaller than expected CP asymmetries, a higher protection level might be important. The neutron flux in BCD may be less than detectors with 4π steradians hadron calorimetry coverage, but BCD has substantial iron in the magnet yokes and muon system. A better estimate of the neutron flux in BCD is needed.

An important design factor will be the hit occupancy. This may ultimately determine the pixel readout system and the highest luminosity possible in the vertex detector. A sophisticated simulation of silicon vertex detector is underway in BCD and will contribute to design considerations in the next couple of months. The pattern recognition strengths of a small pixel device must be traded against the difficulty in manufacturing the electronics for each pixel as the size decreases below 100×100 μm^2.

The following is a list of mechanical issues that the BCD vertex detector group must address in the coming months with simulation and tests. This overall system mechanical design specification is underway. We list issues and raise questions that require examination during this proposal.

1. The vertex detector is envisioned as being constructed with self-supporting modules. The silicon detectors would be glued into a polygon matrix. The modules would then be mounted to an externally supported structure called a "gutter". It is the gutter philosophy and alternatives that require examination during this proposal. Ref. Fermilab TM-1616

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2. The alignment accuracy can be considered in two parts. The initial alignment of detectors with respect to each other and the support structure (the gutter) during and after assembly must be specified. The long and short term drifts due to heating from the amplifiers must be simulated in order to understand the limits of an acceptable tolerance specification. It is estimated the x-y accuracy must be $\leq 4\mu m$, while the accuracy in Z may be $\leq 200\mu m$ over the length of the gutter.

3. The assembly procedure needs to be studied.

4. The cooling requirements may feedback into the electronics design. An efficient cooling system, capable of extracting 2-5 kW of power will permit lower noise amplifier design. The cooling will be gas and liquid.

5. The issue of operating at zero degrees must be studied. This will reduce leakage currents in the detector.

6. Material from connectors and cables are a major source of scattering. Fiber optics should be studied as an alternative signal transfer technique even if power dissipation is higher.

The electronics issues for BCD are similar but perhaps more severe than those for SDE, primarily because of two reasons. First, the required resolution for BCD must be $\leq 10\mu m$. This suggests a pixel size of $\sim 30 \times 30\mu m^2$. The subsequent area available for electronics is roughly an order of magnitude less for BCD than SDE. Secondly, the noise level required is driven by the dipped track problem, ie. small deposition of charge for high angle of incidence tracks. A high efficiency for detecting tracks that deposit $\leq$ 6000 electrons is necessary. Even so, this places a a 45° track cutoff angle of incidence. The remaining issues and questions are listed.

1. A further consideration driving the low noise goals of the electronics, $\sim$ 50 electrons rms noise per pixel, is the very large number of noise hits in a system of $\geq 10^7$ pixels.

2. The radiation damage effects are similar for BCD and SDE, but if BCD runs at higher luminosity, this changes. The higher luminosity running will be determined by the magnitude of the CP asymmetries. Also, the proximity of the silicon to the beam during injection may give large damage, as experienced with UA2.

3. The BCD wishes to readout the vertex detector every few microseconds, in contrast to SDE. The readout design may be different.

4. The resetting philosophy of the pixels for the two experiments may be different. If the reset frequency is too small, pixel occupancy becomes excessive. This may be more severe for SDE if the level 2 wait time is $\geq 50\mu$sec. The reset is important as well to remove dark current build up in the pixels.

5. The bunch crossing tagging procedure must be defined.

6. The advantages of driving analog versus digital signals needs investigation.

7. Centroid finding techniques are of great interest to BCD because the dipped tracks give up to 60 hits.

3.3 High P_t Region and Vertex Detection

Specifically, for solenoidal tracking detectors, a high resolution, radiation hard detector array is needed near the SSC beam to tag b's and τ's and to allow lifetime measurements of new long-lived particles[1]. Such detectors are needed for track reconstruction and accurate dE/dx measurements to search for free quarks in the cores of jets[2]. In addition, the detector provides accurate separation of tracks coming from different primary interaction vertices in a single beam bunch crossing.

The following are some representative physics goals for the vertex detector in the central rapidity region:

1. Tagging of secondary vertices in the search for an intermediate-mass Higgs boson decaying via the $b\bar{b}$ or $\tau\bar{\tau}$ channels. The detector is also valuable for reducing backgrounds by anti-tagging in other Higgs mass regimes.

2. Tagging isolated leptons from W decays to reduce background from QCD jets and photon conversions to e^+e^- pairs. This is needed, for example, to study WW scattering or heavy Higgs decay via the channel $W(\rightarrow l\nu) + W(\rightarrow jets)$.

3. Improvement in signal to noise ratio in high-mass top quark searches. Possible decay chains of interest are, *e.g.*, $t\bar{t} \rightarrow be\nu\bar{b}q\bar{q}$ or $t\bar{t} \rightarrow e\nu\nu b\bar{b}$. The b's may be fairly soft, so the pixel tracker can help here.

4. Accurate measurements of the physics processes involving the copiously produced b quarks.

References

[1] Report of Large Solenoid Detector Group in Proceedings of the Workshop on Experiments, Detectors, and Experimental Areas for the Supercollider, p. 340 (1987).

[2] Exotics Group Summary Report in Proceedings of the Workshop on Experiments, Detectors, and Experimental Areas for the Supercollider, p. 853 (1987).

4 Technical Discussion

4.1 System Design Process

To determine the feasibility of a pixel vertex detector for the SSC several basic questions must be answered:

1. What are the radiation background characteristics in which the vertex detector must operate and how do these background fields determine radiation hardness requirements?
2. What are the physical constraints (*e.g.* multiple coulomb scattering and photon conversion limits, ...) that a vertex detector must match?
3. What are the spatial resolution and track-pair requirements?
4. What are the timing resolution requirements for track tagging?
5. What are the trigger requirements and how do they affect system architecture?
6. What are the data readout requirements and how do they affect system architecture?

The answers to these questions are at least partially known; given this much, then the questions resolve to technical issues:

1. Are high speed, low power, radiation hardened detector and readout assemblies practical with current technology?
2. Can an efficient data collection and processing system be devised which can accommodate these assemblies?
3. Can a stable low-mass mechanical and cooling system be built?

The proposed work addresses these questions from both a technical and a cost viewpoint.

The proposed program will consist of three main activities: the design, simulation, and fabrication of a prototype detector and readout array, the simulation and development of a signal and data processing architecture, and a conceptual design for the entire system. The efforts for the pixel array development are discussed in detail elsewhere, but the prototype design and simulation will influence and be impacted by the work done in the other parts of the proposed effort. For example, the functions and features which will be incorporated into the initial prototype will be those which are necessary to validate the prototype as a proof of concept. These features will be determined by a review of the existing concepts within the team. This task is complicated by the diversity of physical processes investigated by the different collaborators. These concepts will be examined to distill the essential technical features which are common to the various concepts and which will enable a decision to be made as to the feasibility of the pixel array vertex detectors.

With an initial pixel array architecture determined, the question of system feasibility can be addressed. In order to perform this evaluation a candidate system design must be used. From a top down p[point of view, the system must take the information which the detector arrays have collected and determine the trajectories of the particles. The precision with which these measurements must be made is a function of the physics of interest. Representative quantities will be used to arrive at one or more system configurations, from which a design may proceed. The first step in developing a system design is determining a data collection plan. This plan will detail how the data collected by the pixel arrays will be used to accomplish the track reconstruction. This plan will be the roadmap for the signal and data processing design. The data collection plan will address the various trigger configurations so that such quantities as data rates and buffer sizes may be determined. In addition, the data collection plan must address the track reconstruction algorithms. The reconstruction algorithms will influence such system level components as pixel size, number of pixels, signal to noise ratio, and digitization accuracy. By developing such a data collection plan, system architectures may be developed which take advantage of signal preprocess-

ing, thereby reducing subsequent data acquisition and storage requirements. Also, signal processing designs will be investigated which will attempt to reduce other stressing system design requirements such as detector size and number. After the data collection plan is defined a simulation model will be developed which will allow design tradeoff studies to be conducted. The goal of such analysis will be to determine the minimal system configuration necessary to achieve the physics goals.

Finally, a complete system design will be performed to assess cost and lifetime considerations. The system design will cover mechanical packaging, detector layout, cabling, cooling, shielding, and other matters that need to be studied to identify technology and cost drivers.

The 1st phase 12 month program proposed herein is shown in Figure 2. Provision is made for regular technical interchange meetings at 2 and 3 month intervals with all principal members of the team involved in pixel detector development. The proposed readout design will be thoroughly reviewed at a concept design review, preliminary design review and final design review before initiating wafer fabrication. This review process will assure that the critical readout requirements necessary to demonstrate technical feasibility for both the BCD and SDE experiments are being addressed.

A number of readout designs have been proposed (Ref1-7) and these will be thoroughly analyzed so that feasibility can be assessed:

4.2 Design, Fabrication, and Test of a Prototype Pixel Detector

The objective of the fabrication task is to fabricate prototype detector arrays who's performance can be measured and compared against SSC goals. Experience gained in the prototype development will then be utilized in the development of the full scale system.

Following the development of the conceptual design described in the pre-

vious section, a detailed design must be produced. The detailed design development comprises two broad areas of activity, technology selection and circuit development. There are several device technology candidates which could be utilized in the development of a prototype array. Technology selection involved quantitatively trading the strengths and weaknesses of each available technology off against the readout requirements. Silicon MOS technology offers very low power and reasonably high speed. It is inherently hard against neutron radiation, and can be hardened against total dose radiation. Bipolar technology offers speed advantages over MOS, but at the expense of somewhat higher power. Bipolar devices are extremely hard to total dose but suffer some degradation in neutron environments. Unipolar devices, such as JFETS and MESFETS, offer further speed enhancements when fabricated in high mobility material such as gallium arsenide. Their radiation hardness is similar to that of bipolar transistors. Finally, it may be desirable to employ a BICMOS process, which is a merger of MOS and bipolar technologies on the same chip.

This allows the use of low power MOS circuitry in power critical areas, while having bipolar transistors available for portions of the circuit which require high drive capability.

Circuit development is composed of several distinct activities. A schematic must be defined which implements the full functionality of the candidate architecture. A specific process for readout fabrication must be selected, and device parameters input into the circuit simulator. The circuit simulator is then used to optimize the circuit design, and to predict the circuit performance in the areas of interest, such as power dissipation, radiation hardness, noise, and speed. The following requirements were agreed upon for the first prototype hybrid pixel readout. These requirements were considered generic to both the SDE and BCD experiments. They are appropriate for a first year demonstration to demonstration to demonstrate the technical feasibility of pixel detector arrays;

1. Power from 100 mw per square centimeter to 1000 mw per square centimeter.
2. Readout time approximately 1 microsecond

3. Tag time about 10 nanoseconds
4. Radiation hardness 1/2 megarad
5. Noise level of 200 noise electrons

Following the optimization of the circuit schematic, the circuit is laid out using computer-aided design tools.

All of the elements of the technology selection and circuit development activities are interrelated, and therefore cannot simply proceed in a sequential fashion. For example, the circuit density of a given technology dictates how complex a circuit schematic can be accommodated in a given unit cell area. Likewise, device parameters and parasitic element values specific to a given process will affect both the detailed circuit schematics as well as the predicted performance. Therefore, the detailed design process is an iterative one, with each iteration developing more and more design detail. In our experience, the design process usually converges within two to three iterations.

Following the completion of the final layout, photoplates are fabricated. These photoplates are then used in conjunction with the chosen process to fabricate the prototype arrays. Depending on the process chosen, the readout ic 's will be fabricated either at a Hughes facility or at an outside foundry. The fabrication process generally takes 8-12 weeks. After fabrication, the finished wafers are returned to HMC for testing.

The completed prototype arrays will be subjected to a variety of tests in order to verify their performance. Initially, the readout ic's, are tested at the waf er level in order to determine whether the design is functioning correctly, as well as to identify candidate parts for dicing, packaging and performance testing. Following wafer level testing, candidate parts will be hybridized to detectors and packaged for performance testing. The devices will be operated at speed using a pulsed laser as an excitation source. Such a setup will enable a full range of diagnostic and performance testing to be performed.

Following the diagnostic testing and performance verification, parts will

be delivered to the appropriate university and laboratory researchers for HEP tracking experiments.

5 Technical Progress Summary

6 Statement of Work and Budget Summary

The following statements of work and budgets for the various team activities are proposed.

6.1 Hughes Aircraft Company

1. Hughes Aircraft Company budget request -$480K
2. Perform system level architecture and design studies for pixel detector systems, for vertex tracking for both SDE and BCD pixel experiments;
3. Perform a preliminary cost analysis of the proposed pixel detector systems;
4. Design fab and test pixel array addressing the critical requirements for technical feasibility.

6.2 Lawrence Berkeley Laboratory

1. Lawrence Berkeley Laboratory budget request - $225K
2. Complete the design and testing of a nonrad hard prototype of the LBL smart pixel concept;
3. Continue development work on LBL detector process to provide appropriate pixel detector arrays for Hughes Aircraft Company;
4. Perform analysis of radiation damage studies on detectors, circuitry, and hybrid arrays with other collaboration members;
5. Provide design support and system analysis to Hughes Aircraft Company including a review of proposed designs.

6.3 UC Berkeley - Space Sciences Laboratory

1. UC Berkeley - SSL budget request - $180 K
2. Continue testing of the current pixel arrays that have been prepared;
3. Digital signal processor (DSP) design;
4. Test system development.

6.4 Stanford Linear Accelerator Center

1. Standard Linear Accelerator - $40K
2. Perform radiation and beam tests with the current pixel arrays and those

   being developed;
3. Perform mechanical and cooling studies of proposed vertex detector systems.

6.5 University of Oklahoma, Yale University, and University of Iowa

1. Budget request - $85K
2. Radiation Damage Studies;
3. Beam tests at Fermilab;
4. Preparation for Beam Tests of a Vertex Detector Subsystem.

6.6 UC Davis and Iowa State University

1. Budget request - $40K
2. Physics simulations of system performance in SSC environment;
3. Proton beam testing of pixel detector arrays.

6.7 University of Pennsylvania, Princeton University

1. No funding requested;
2. Provide design analysis and simulation for BCD experiment.

Total: $1050K

7 Budget Plan

8 Appendices

8.1 Status of Pixel Development

8.2 Hughes Aircraft Company Experience in Pixel Array Development

8.3 LBL Experience in Detector and Circuit Development

8.4 UCB/SSL Experience in Pixel Array Utilization