A Level 1.5 Trigger for the
Upgraded Belle SVD

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1 Introduction

An important conclusion of the Belle SVD/CDC Task Force\textsuperscript{1} is that the upgraded SVD should provide Level 1 trigger information. This information will be used to select events with \( z \) vertices close to the nominal IP.

One way to accomplish this is to add discriminators to the VA chips, whose outputs could then be used to form a trigger signal. This approach is straightforward in principle, but involves development of a new chip (the “VATA”). Although chips similar to this have been successfully produced by IDEAS already, the deployment of the VATA represents a departure from our existing philosophy of having no active digital lines prior to the receipt of the Level 1 trigger.

In this note I propose an alternate strategy for implementing a \( z \)-vertex trigger that uses information extracted from the external readout electronics during the analog scan. This approach makes use of existing 0.35 \( \mu \)m VA1 chips\textsuperscript{2} and does not require significant R&D. Thus it can be ready for installation in the summer of 2002.

The basic idea is to extract trigger information during the scanning of the analog multiplexers of the VA1 chips. This can be done by replacing the front-end analog “mezannine boards” of the Halny boards with modified versions that incorporate additional field-programmable-gate-array (FPGA) logic between the FADCs and the FIFO input buffers\textsuperscript{3}

The advantages of this approach include:

- No new chip development is needed, meaning that a summer 2002 deployment of the full five-layer SVD is possible (Option 1 in the Taskforce Report).

\textsuperscript{1}The Taskforce Webpage is http://bsumsrv1.kek.jp/~svd/private/tfocdsvd/

\textsuperscript{2}We may choose, however, to resubmit the VA1 0.35 \( \mu \)m to obtain an epitaxial layer, which is known to mitigate single-event-upset effects.

\textsuperscript{3}It remains to be seen whether the additional circuitry would fit on the mezzanine boards. If not, it would be necessary produce a set of modules dedicated to the task. This, however, is not a fundamental problem.
The on-detector electronics would be essentially the same as what we now have. In particular, there will be no digital activity on the hybrids prior to the level 1 trigger.

The trigger-bit extraction logic can implement pedestal subtraction and clustering, meaning that the information used in the level 1.5 trigger would be of near offline quality. This would not only result in better trigger performance, but would also simplify the task of determining the trigger efficiency at the time of offline analysis.

By allowing more time to make a trigger decision, it is possible to implement more sophisticated logic, opening up the possibility of obtaining higher rejection factors, thereby lightening the load on the downstream DAQ.

The principal drawback is the time required to complete the scan, which results in an irreducible deadtime. For a four-chip (512-channel) hybrid read by a single Halny channel at a scan rate of 200 ns per channel, the time required is about 100 $\mu$s. This would produce 10% deadtime for an input trigger rate of 1 kHz. However, by incorporating two or four FADCs on the modified analog input board, this time could be reduced to 50 $\mu$s or 25 $\mu$s. The latter time yields a 2.5% deadtime at a 1 kHz trigger rate.

2 Design Details

2.1 Trigger Bit Extraction

The readout of the VA1 chips starts with a serial scan of the analog outputs of the track-and-hold circuits implemented on the VA1s. In the present scheme, the data pass from the on-chip multiplexer outputs, through the repeater system, where they are buffered and transmitted through $\sim$ 30 m cables to the analog inputs of the Halny boards. The digital output of an FADC on the Halny boards is then fed to a derandomizing FIFO that sits between the FADC and the DSPs (see Fig. 1a). By inserting a field-programmable gate array (FPGA or “Xilinx”) between the FADC and the FIFO (see Fig. 1b), it will be possible to identify strips or strip clusters with above-threshold energy depositions. This information is then used to set trigger bits, corresponding to the OR of groups of 32 strips. The logic required to do so is straightforward, consisting of digital circuitry to subtract precalculated pedestal data followed by a digital comparator to apply a threshold (see Fig. 2). RAMs implemented in the FPGA can be used to store channel-by-channel pedestals and
thresholds. If cluster-finding is desirable a three-stage pipeline adder can be used to compute a moving sum, as shown in Fig. 3.

Data from the ADC pass through the FPGA unaltered and are routed to the DSP. The DSP then applies the standard processing. As noted in Section 1 it may prove desirable to scan the four chips on each hybrid in parallel. In this case the FPGA will need to combine the four ADC output streams into a single stream to be read by the Halny's DSP. Indeed it may even prove desirable to combine two four-chip hybrid streams into a single Halny channel, although this option would require further study. In particular, it would require reducing the Halny processing time by a factor of two, which would require a simplified zero-suppression algorithm.

2.2 Board Counts

In what follows we assume that the system has about 256 four-chip hybrids and that each Halny channel handles four VA1s.

Maintaining a one-to-one correspondence between Halny boards and analog input boards dictates that each analog input board will need to handle 4 VA1s × 4 channels = 16 analog signals. This will require higher density analog-input connectors than are currently in use. There will be a total of 64 input boards.
Figure 2: Logic used to extract trigger information. Only single strips are considered.

Figure 3: Logic used to extract trigger information. This somewhat more elaborate version applies a threshold to a cluster of strips.
Each of the 16 channels on an input board will produce 4 bits of trigger data, for a total of 64 bits. These could either be read in parallel as a single 64-bit word or serially as a sequence of four (say) 16-bit words. The latter approach would lead to a tidier system layout (fewer cables), but the latter would be needed to maintain compatibility with a level 1 trigger scheme, where all trigger bits would necessarily need to be transferred in parallel.

If all five layers participate in the trigger, then there will be approximately 4K trigger bits. If these are transferred in eight time steps, then the number of physical interconnects (wires) will be reduced to a more manageable 500. For example, if the trigger boards can accommodate 64 inputs the number required would be eight. This assumes that the trigger logic can accommodate such a high density of inputs (each of the boards would deal with $8 \times 64 = 512$ inputs), which is a question for further study.

If the *Halny* algorithm can be simplified to the point where the zero-suppression can be done in less than 2 ms for eight VA1’s (only a $\sim 10\%$ reduction relative to the current value 1.4 ms for five VA1s) then it should be possible to accommodate all 1000 VAs with the current set of 32 *Halny* modules.

The module counts are roughly summarized in Fig. 4.

## 3 Level 0 Trigger

One loose end that must not be forgotten is the need for a Level 0 pretrigger signal to trigger the T/H circuits of the VA1. This is needed in either trigger scheme.

Currently this signal is formed from a coincidence between TSF and TOF counters. Since each Level 0 generates approximately 2.5 $\mu$s of deadtime, the Level 0 rate should be ideally kept below 4 kHz or so (this would give 1% deadtime).
If the VATA scheme is adopted, then it is natural to contemplate placing the SVD in coincidence with the ToF to lower the Level 0 rate. However, it should also be possible to use the newly proposed small-cell inner layers of the CDC (CDC SC). The basic idea is illustrated in Fig. 5.

To be worth the effort, the added requirement must reduce the Level 0 rate by a factor of ~four or more. In other word, a hit in the CDC SC layer should be be present for no more than 25% of the TOF-TSC fires. Thus

$$p_{CDC-SC} \simeq R\Delta T \leq 0.25$$

where $R$ is the rate of a CDC-SC $\phi$ segment and $\Delta T$ is the resolving time. For a 2.5-mm drift the charge collection time is $\sim 50$ ns. Doubling this to $\Delta T = 100$ ns yields $R_{\text{max}} = 2.5$ MHz for a CDC-SC $\phi$ segment. To maintain full acceptance, such a segment would need to cover approximately $1/8$ of $2\pi$ so that the total rate for the layer could be as high as 20 MHz. If higher rates are thought to be likely, one would need to include inner layers of the CDC proper.
4 Implementation Roadmap

One of the advantages of this approach is that it would allow us to proceed without extensive chip development. However, a number of steps would need to be taken regardless of what trigger scheme is adopted.

- Refabricate the 0.35 μm ICs with an epitaxial layer. There is quite a bit of anecdotal evidence that this reduces the sensitivity to SEU and SELU.

- Redesign the hybrids to add extra analog signal output lines. If we decide to go with two channels per hybrid (two extra lines) the redesign is minimal and will have little impact. If we decide to go with four channels per hybrid (six extra lines), a more extensive redesign is needed. Indeed, this approach might require the use of on-chip DACs for bias settings, although another option would be to design a separate small chip to implement these functions.

- Redesign the REBO system. Here there are two options:
  
  - Go back to the ABC scheme, placing simple cards with voltage regulators and buffering at the position of the current repeaters.
  
  - Implement on-chip biasing controlled through a serial interface. As noted above, this could be done either through a redesign of the VA (as in the VATA) or by designing a separate chip for the purpose.

- Build the front-end analog boards with trigger pickoffs. These would probably be implemented in 9U VME.

- Modify the Halny modules to accept digital inputs. This would require us to replace the mezzanine boards and the front panels. The replacement mezzanine boards would be quite simple, although it may be difficult to find the stacking connectors since the parts used for this purpose do not appear to be completely standard.

Another possibility worth considering is the use of commercial DSP modules. Although this option would certainly be more expensive, it would be less manpower intensive, especially in comparison to a project wherein we would need to build additional Halny modules.

Fig. 6 shows a timeline for the completion of this work.
### Figure 6: Rough schedule for implementation of the five-layer SVD, assuming that the scheme proposed herein is adopted.

### 5 Discussion

The attraction of this scheme is that most of the development work required involves reasonably straightforward (famous last words?!) off-detector electronics. Furthermore, with the exception of the analog input boards, most of the new electronics is needed in any five-layer scheme. The analog input boards require minimal development work since we could take full advantage of the Halny front-end design. They would require a simple VME interface, but once again an existing scheme could be used.

It is also possible to view this approach as a backup scheme. Indeed that was my original proposal. However, given the shortage of manpower it is not clear that enough effort would be expended to really make this work in that scenario.