VA1TA Belle at Ideas

HTA (Tokyo Univ.), DMA (Princeton Univ.), SIM, JAT, KYO

Jan 22, 2001

Agenda:

1. VA1TA: Status / Design Review / Schedule
2. VA1TA: Hybrid
3. VA1TA: Evaluation Board
4. Order and Invoice Status

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1. VA1TA

DaM: Digital Output (ta, tb)

SIM: Schematic Capture and Electrical Simulation of the Top Level being done. Some tuning left.

a) VA Preamplifier Output buffer, higher bandwidth => higher VA amplitude

VA output buffer => better linearity

Current Compensation with Fixed Resistor: 2xR 1.5-2mm length.

Preamplifier output buffer: 200uW increase in the power consumption per channel.

TA trigger width at 100nsec.

[TA power consumption: *************]

Dummy channel => Vfp, Vfs, Vref, VfsF generation.

b) VA Biases:

PreBias: 300uA ± 150uA (3bits)
ShaBias: 22uA ± 9uA (3bits)
Ibuf: 140uA ± 60uA (3bits)
Vfp: To be determined (3bits)
Vfs: To be determined (3bits)
BufBi: 50uA. No DACs.

Ta Biases

VfsF: To be determined (3bits) (2 sets of 3 bits in parallel: 75ns or 300ns)
Sbi: 70uA ± 30uA (3bits)
OtaBias (Obi): 90uA ± 30uA (3bits)
TwBias: 100ns (nominal width). Bias to be determined. 3 bits DAC.
Vrc: Nominal value to be determined. Bias to be determined. 3 bits DAC.
Vthr: 2000-8000 e-. Nominal threshold at 5000e-. 5 bits DAC.
Noise level at 800e-.

JAT Obs: 75ns: 10mV/fC; 300ns: 12mV/fC
Threshold Trimming DACs: 4 bits. Threshold Spread <400e-
Main Bias: 500uA.

c) Serial Register (RegIn)

CtrlReg: 5 bits
TrigMask: 128 bits
Thr TrimDACs: 512 bits
BiasDACs: 35 bits

Total 680 bits

d) SEU Scheme

Signal out: SEU Detected:

Majority: valid bit from the register.

Correction feedback: If SEU => Majority copied to the latches automatically.

Readback function implemented.

OBS: during the latch loading the correction feedback is disabled.

SEU Detected output: single open drain. Quiescent output: zero current. 1usec pulse. 100uA pulse.

EPITAXIAL LAYER and Substrate Contacts.
e) **Schedule**

Feb 15: Submission (VA1TA, VA1'', VA32TA)

Apr 15: Chips back from foundry: 8 weeks after submission.

1600 VA1'' tested (AMS engineering run)
1600 VA1TA

Following contract for chip testing...

Internal Evaluation: VADAQ and test board.

Apr 28: Test results.

Sep 30: Hybrid production deadline (1st delivery).

Oct 1: Ladder production.

VA1'' backup for VA1TA.

2. **Hybrid (VA1TA)**

4 chips; candidate connector: **Connector Drawing with KYO**

dimension same as 4 VA1''. VA1TA length: $\approx 8.4$ mm (4.95 mm)
capacitor $V_{fp}$, $V_{fs}$, Prebias, Shabias, etc **removed**.
4 chips read out in parallel.

4 layers with 51 pin connector; innermost layer (12 hybrids) with 37 pin connector

Signals at connector (51 pin connector – dual row nanonics, 5.7 mm long + solder area = 7.2 mm.)

<table>
<thead>
<tr>
<th>Pin</th>
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<tbody>
<tr>
<td>4x2 (outa, outb)</td>
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<tr>
<td>4x2 (ta, tb)</td>
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<tr>
<td>1x1 (RegIn)</td>
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<tr>
<td>1x1 (ClikIn)</td>
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<tr>
<td>1X1 (RegOut)</td>
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<tr>
<td>1x1 (ShiftInB)</td>
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<td>1x1 (Ck)</td>
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<tr>
<td>1x1 (CkB)</td>
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<tr>
<td>4x1 (ShiftOutB)</td>
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<tr>
<td>1x1 (Hold)</td>
</tr>
<tr>
<td>1x1 (HoldB)</td>
</tr>
<tr>
<td>1x1 (Reset)</td>
</tr>
<tr>
<td>1x1 (ResetB)</td>
</tr>
<tr>
<td>1x1 (Cal)</td>
</tr>
<tr>
<td>1x1 (Mbias)</td>
</tr>
<tr>
<td>1x1 (SeuB)</td>
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<tr>
<td>1x1 (Load)</td>
</tr>
<tr>
<td>1x1 (ReadBack)</td>
</tr>
<tr>
<td>1x1 (DetectorBias)</td>
</tr>
<tr>
<td>1x1 (Vthr)</td>
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<tr>
<td>1x1 VfsS</td>
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<tr>
<td>1x1 VfsF</td>
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<tr>
<td>1x1 (DVDD)</td>
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<tr>
<td>1x1 (DVSS)</td>
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<tr>
<td>1x1 (DGND)</td>
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<tr>
<td>1x1 (AVDD)</td>
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<tr>
<td>2x1 (AVSS)</td>
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<tr>
<td>6x1 (AGND)</td>
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- **a)** Signals not used in the innermost layer hybrids.
- **b)** Baseline for not populated area: last 4 VA1'' HYBRID. OBS: Decoupling caps not needed ($V_{fp}$, etc).
- **c)** Jumpers for $V_{thr}$, $V_{fs}$ and $V_{fs}$ to Power Supplies.
- **d)** 2 stage design: FR4 and Kyocera.
- **e)** **Sketch of the Pin Out Diagram**
Schedule:

Mar 1:  FR4 CDR at Ideas.
Mar 24:  FR4 hybrid submission to production.
Apr 15:  FR4 hybrid production finished
Apr 28:  FR4 hybrid tested.
May: 20 FR4 hybrids (all). 5 with load capacitance (4 x every other channel).
Jun 1:  Submission of Kyocera design.
Sept 1:  Kyocera delivery to Ideas.
Sept 30:  Ideas start delivery of ceramics to Belle.
> 30 ceramics/week. Total 360 ceramic hybrids.
Dec 31:  All delivery done (>260).

• OBS: In case of single chip tested test board, send 10 boards to Tajima-san.
• Big capacitors (22uF/6V and 1uF/100V) being searched by Tajima-san, but PEG should not give up on his search. To be ordered as soon as possible.

3. VA_DAQ 4 VA1TA:

• VA1TA Power Supply: +1.5V and –2V.
• Adapter board with MUX for separate analogue output from the chips
• Wire OR trigger outputs.
• FPGA at adapter board to control the Mux.
• Load ---
• ReadBack ---
• Trigger Out from Adapter Card, Trigger Into the Adapter Card for HOLD.

Schedule:

• April: Ready.

4. Invoice Status

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Send Invoices to Princeton: Production and Testing of VA1TA,
Evaluation Board,
FR4 Design and FR4 Production.